

# Avago RF VMMK Devices Improve Performance by Reducing Parasitic Inductance and Capacitance



## White Paper



### Abstract

Packaging has always significantly impacted on microwave IC and amplifier performance. In most cases, the inherent parasitic capacitance and inductance of the package lead frame and wire bonds set a limit to circuit performance. Avago Technologies developed a bonded-wafer-to-wafer package technology in 2004 and now offers innovative microwave gallium arsenide (GaAs) VMMK devices based on the proprietary WaferCAP™ chip scale package. Surface-mount (SMT), very low cost VMMK amplifier and FET devices are available today and soon to be released diodes and detectors will be added to the VMMK series.

### VMMK Devices and Wafer-Level, Chip-Scale Package Technology

As shown in Figure 1, VMMK devices benefit from Avago's WaferCAP technology that eliminates the losses and parasitic circuit elements of conventional RF SMT packages. By eliminating wire bonds and package leads and their stray inductance and capacitance, a low-loss low-impedance signal path is made for the chip and package system.

The air cavity has a low dielectric constant (air) above the active device to allow high-frequency operation. In addition, it provides mechanical protection for the device during use. As shown in Figure 2, all inputs and outputs are routed through via-holes to the backside of the device wafer, eliminating performance-limiting wire bonds. Proprietary metallization and sealing technology allow standard solder surface mount pick, place, reflow, and wash.

Eliminating wire bonds and improving thermal characteristics increase WaferCAP reliability over that of conventional SMT package technology.

WaferCAP technology and its benefits come without users installing any new manufacturing and assembly equipment or processes. Existing tooling for standard SMT assembly and handling is adequate. High volume "pick and place" or "chip shooter production equipment are compatible with Avago WaferCAP RF components.

Finally, by eliminating package pins, lead frame, wire bonds and molding compound, RF WaferCAP devices are thinner, weigh less and need less PCB area than most conventional RF SMT devices. For example, a VMMK-2x03 RF amplifier (1 mm x 0.5 mm x 0.25 mm) needs just 5 % of the volume and 10% of the PCB area required by a standard SOT-342 package. Compared to many standard RF SMT packages, VMMK device PCB savings will be at least 50%.

Along with significantly reduced parasitics, WaferCAP devices directly connected to PCB traces, resulting in reduced RF signal path and essentially no RF loss. The air cavity formed above the RF chip by the cap wafer also reducing parasitics and improves performance.

Enhanced heat transfer is inherent in Avago WaferCAP technology. Close contact to the PCB improves heat transfer as does the smaller mass.

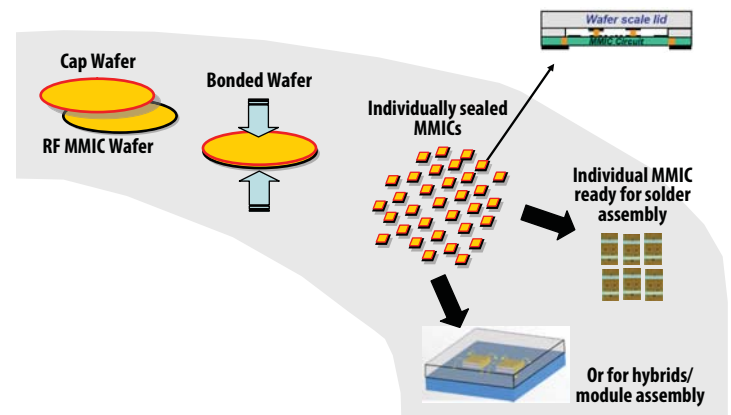


Figure 1. WaferCAP process uses low cost semiconductor process

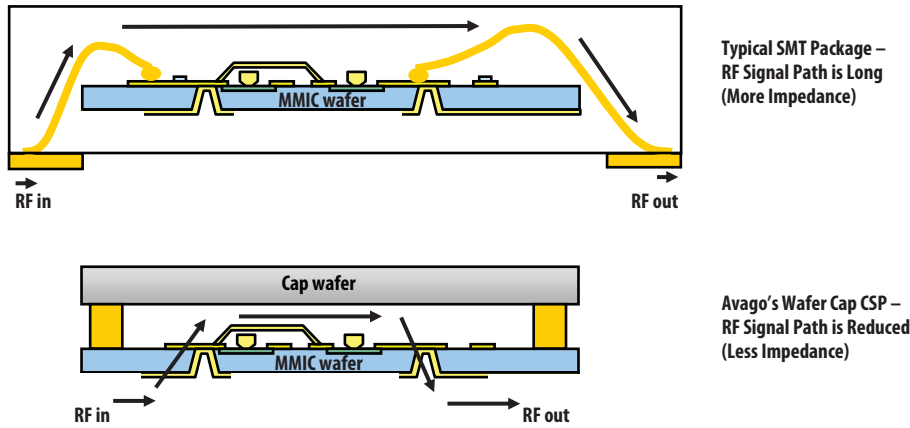
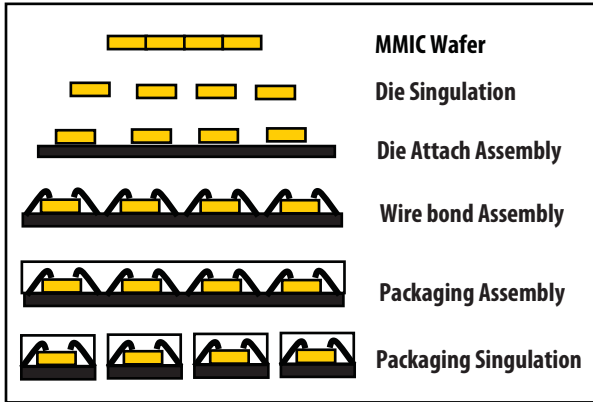


Figure 2. WaferCAP technology reduces RF losses and parasitic inductance and capacitance

**Typical Assembly Process of Plastic Packaged Product**



**Assembly Process of Avago's Wafer Cap Product**

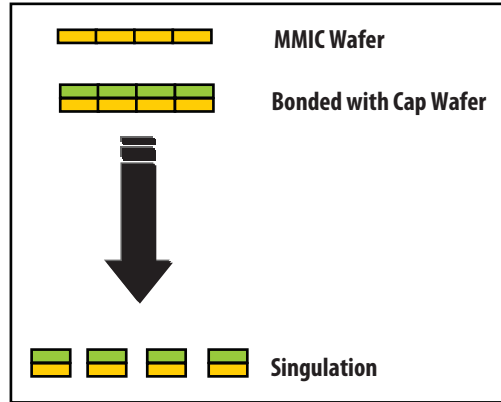


Figure 3. VMMK devices are low cost and suitable for high volume RF applications

**Unmatched Benefits at Low Cost**

MicroCAP technology takes advantage of Avago's high volume semiconductor manufacturing capability. As shown in Figure 3, by eliminating the costly steps needed in conventional SMT assembly, such as wire bonds, die attach and SMT molding, Avago's WaferCAP VMMK parts feature superior performance at a low cost. VMMK devices are very small; twenty VMMK devices will fit inside the tiny SOT-343 package, as shown in Figure 4.

**Simple Assembly and Product Manufacturing**

No extra ordinary PCB design, manufacturing or assembly processes are necessary for users to benefit from VMMK device performance. Avago VMMK components will easily fit into any design suitable for SMT technology by following a few simple design and layout cautions.

**Standard PCB Material**

VMMK devices have been qualified with FR4 (10 mil maximum thickness) material with one ounce copper for both top and bottom metal. Low loss microwave substrates such as Rogers 5880, RO4003 and RO4350 have a coefficient of thermal expansion (CTE) similar to FR4 material and are also acceptable.

Soldering onto material with greater thermal expansion than FR5 or high glass transition temperature (Tg) FR4 should not be used.

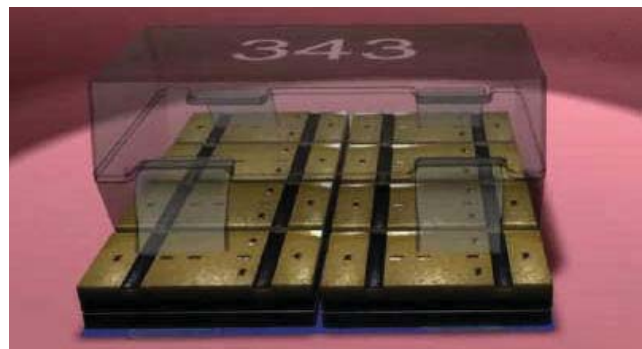


Figure 4. Twenty VMMK packages fit inside a SOT-343 package

## PCB Tips and Cautions

VMMK devices have a form factor **similar** to that of a standard 0402 capacitor. However, it is important that PCBs designers *do not use a standard 402 land pattern for Avago VMMK parts*. The visible VMMK metallization is not necessarily the “solderable” area. Refer to each product data sheet for the proper VMMK land pattern; an example is shown in Figure 5.

A solder resist layer, or solder stop, should surround the pads to inhibit solder bridging. The gap between the pads must not be bridged with solder. Pad material is minimum 5.0  $\mu\text{m}$  thick Au under maximum 1.0  $\mu\text{m}$  thick Ni with Au flash. When liquid solder is present, the Au flash dissolves and the Ni layer becomes wetted to the liquid solder. This occurs during the solder reflow process when attaching the device to the PCB.

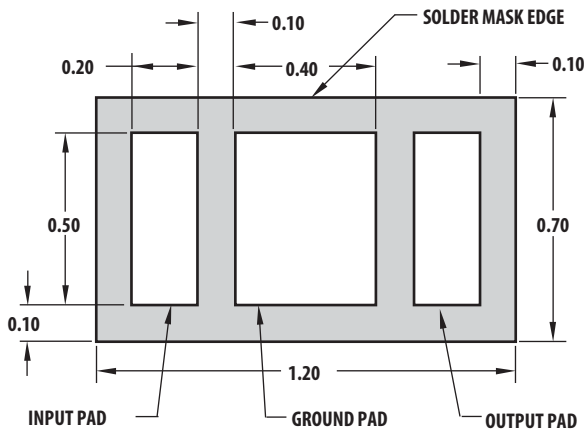
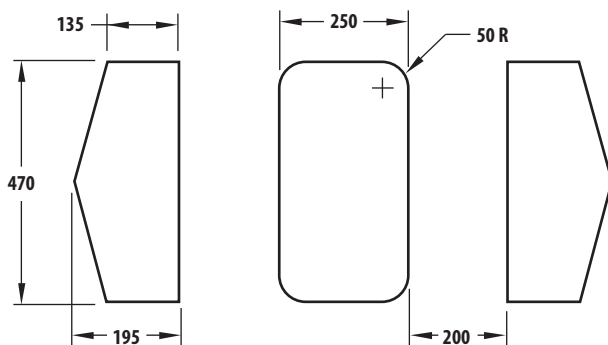


Figure 5. VMMK land pattern



Note: Dimensions in microns

Figure 6. Suggested laser cut stencil pattern (100 micron thick).

Some easy to follow, best practice guidelines will prevent problems in manufacturing and assembly:

1. There should be no uncapped via holes under the PCB solder pad. Open vias should be blocked from the solder pad by a solder mask to avoid solder flow into an open via.
2. The solder stencil should ensure the proper amount of solder paste is deposited on the solder pads. A stencil pattern for the VMMK devices is shown in Figure 6. The angled outer edges help fill the stencil if the squeegee pass is slightly off axis. Additional attachment information can be found in Avago AN- 5378.
3. VMMK devices can be cleaned with standard aqueous cleaning procedures using DI water. Ultrasonic cleaning and vapor phase cleaning should not be used.
4. VMMK devices use a standard BCB polymer as a gasket material. BCB polymers have been used historically for die passivation, and semiconductor application with exposed surface such as flip-chips and wafer level chip packages. Good practice is to check with the PCB manufacturing and assembly house to verify that the Dow Chemical BCB polymer used in VMMK devices is compatible with their processes. Additional information can be found in Avago AN-5378.
5. PCB footprints are given in each device data sheet and AN-5378 has additional guidelines. However, in general, modeling and actual tests indicate that placing plated through holes adjacent to and on either side of the device provides adequate grounding.
6. Solder pastes with no clean or water soluble flux are recommended. Avoid conductive epoxy as shorts can develop.
7. Avago VMMK devices have a moisture sensitivity level of MSL2a. Bake the products if the MSL2a requirements have not been met.

## System Package Considerations and High Volume Assembly

Avago VMMK devices have not been designed for or qualified for over-molding or encapsulation. Molding pressures may compromise the GaAs circuit cavity and damage the device. At a minimum, electrical performance could be impaired.

VMMK devices can be handled by standard high volume PCB assembly equipment. Several chip shooters, operating with standard settings and nozzles, have been evaluated and give good results. The Zuki KE-2050RL and the Panasonic MSF NM-MD15 have been used successfully.

## Solder Reflow Process and Guidelines

The infrared/convection reflow profile investigated and recommended for VMMK parts is based on JEDEC/IPC standard J-STD-020 revision C. VMMK devices have been qualified to withstand a maximum of three cycles of solder reflow according to the conditions of J-STD-020C. Further reflow would degrade the die metal interface with the solder. This device has not been designed or qualified for wave soldering or vapor phase reflow. These processes should not be used.

The recommended and most common reflow method is a belt furnace using convection/ IR heat transfer. By following the J-STD-020C standard and adhering to a few guidelines, the reflow soldering of VMMK devices should be trouble free. General guidelines to remember when reviewing a reflow soldering process are:

1. Avoid a prolonged hot preheat as excessive oxidation can occur. The time over 217°C is critical and will determine the appearance and integrity of the solder joint after reflow. Longer reflow time may result in excessive inter-metallic growth, dull and gritty solder joint appearance, and charring of flux residues. Time below 30 seconds may result in insufficient wetting and poor intermetallic formation.
2. In general, VMMK devices should be exposed to only the minimum lead-free process temperature and times necessary to achieve a uniform reflow of solder. The timing and rates for the ramp-up and cool-down zones, as specified in the J-STD-020C standard, are low enough to not cause board deformation or damage VMMK devices by thermal shock. The standard's reflow temperature is low enough to avoid damaging the internal VMMK circuitry during solder reflow operations provided the time of exposure at peak reflow temperature is not excessive, as per the JEDEC standard.

By following the JEDEC standard and these guidelines SMT reflow soldering of VMMK devices should be trouble free. Detailed solder reflow information is available in the Avago AN-5378 application note.

## Summary

All VMMK devices are manufactured using Avago's proprietary WaferCAP technology. By greatly reducing parasitic capacitance and inductance of the package, VMMK devices offer excellent performance in a compact package and at low cost.

By following a few easy to implement PCB layout and design guidelines, and after reviewing current SMT manufacturing processes for J-STD-020C compliance, VMMK components will fit high volume, modern SMT assembly processes.

Amplifiers and FETs are currently offered in the VMMK series. Avago new product plans for the VMMK series include more amplifiers as well as the addition of diode and detector devices. Future parts will have more complex functionality and increased pad count, but the basic advantages of miniaturization, excellent RF performance and low cost will always be the main advantages of VMMK devices over conventional SMT packaged RF devices.

For product information and a complete list of distributors, please go to our web site: [www.avagotech.com](http://www.avagotech.com)