

# A High Isolation Buffer Amplifier using Enhancement Mode PHEMT Technology

## White Paper

### Abstract

The design and implementation of a high isolation buffer amplifier is presented. This IC uses a two gain stage topology processed in the Avago Technologies Enhancement Mode pHEMT GaAs technology and is packaged in the 8-lead 2mm x 2mm LPCC. It operates preferably from a 5 Volt supply and consumes approximately 35 mA quiescent current. By varying an external bias resistor, the buffer amplifier can deliver maximum output power up to 20 dBm at 2 GHz. It has better than 40 dB of input-output port isolation and operates from 0.5 GHz to 6 GHz. The IC features input and output ports matched to 50 ohms impedance and provides 20 dB compressed gain at 2 GHz. A typical use of the part is for driving a passive mixer LO port from a VCO where high reverse isolation is required by the VCO.

### Introduction

Modern radio receivers must be capable of selecting one of several transmitted signals within their operating frequency range without interference from any other. This characteristic is commonly referred to as selectivity. The super-heterodyne radio architecture addresses this need by implementing one or more mixers to down-convert the desired incoming radio signal to a fixed intermediate frequency. At this point filtering and amplification can be accomplished in preparation for detection. An example of the typical radio architecture is depicted in Figure 1.

Frequency conversion is accomplished by beating the incoming radio frequency (RF) signal with a stable local oscillator (LO) signal, thus producing the desired intermediate frequency (IF). Much of the system's performance and utility is traceable to the frequency stability of the LO signal.

A voltage controlled oscillator (VCO) generates the required LO signal at low power levels (0 dBm) and

is easily frequency pulled by variations in load impedance. High linearity passive mixers typically require +17 dBm LO drive levels and present varying load impedances to the LO source. Hence, a need exists for a buffer amplifier that can raise the VCO output signal to the required power level of the mixer, while isolating the VCO from the mixer's varying port impedance.

This paper describes a variable gain, two-stage, high isolation amplifier with a maximum output power of 20 dBm. It is suitable for use in a variety of buffering applications.

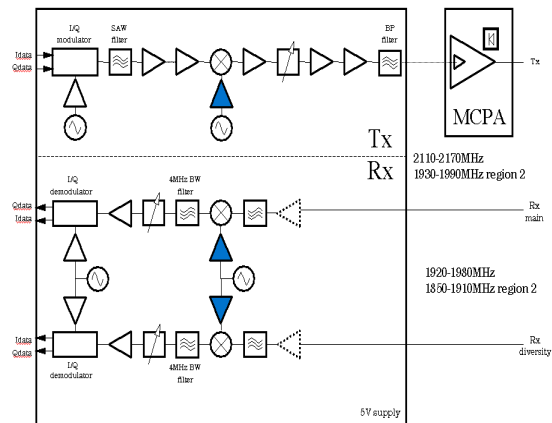


Figure 1. LO buffer amplifier in superheterodyne WCDMA transmitter and receiver system.

### Circuit Design

Depletion Mode GaAs FETs have dominated the microwave and RF business for many years. Advances by internal Avago Wireless Semiconductor Division R&D have enabled the development of a high performance enhancement mode pHEMT device technology that does not require negative bias voltages for its operation<sup>[1]</sup>. This technology maintains the advantages of high linearity and low noise of pHEMTs while eliminating the need for additional negative voltage generation circuits<sup>[2]</sup>.

The design of this amplifier uses a 2-gain stage topology as shown in Figure 2. The first stage is a common-source amplifier biased by a current mirror. High gain is enabled through the use of a current source load. Feedback is used to achieve input impedance matching. The second stage is also a common-source amplifier biased by a current mirror. It uses an external inductor as a load to achieve high output voltage swing and thereby, larger output drive capability.

The typical compressed gain of this design is 20 dB with 65 mA current consumption at compression. It has more than 40 dB of input-output port isolation at 2 GHz and operates from 0.5 GHz to 6 GHz. Maximum output power is 20 dBm and can be varied with an external bias resistor.

### Layout and Packaging

Figure 3 is the photo of the amplifier. The die measures 525µm x 760µm. It is fabricated on a 6 inch diameter wafer utilizing AlGaAs technology.

This design is packaged in a low-profile 2 mm x 2 mm LPCC package. This package is a thermally efficient leadless package offering excellent RF response over wide operating frequency range from DC to 6 GHz.

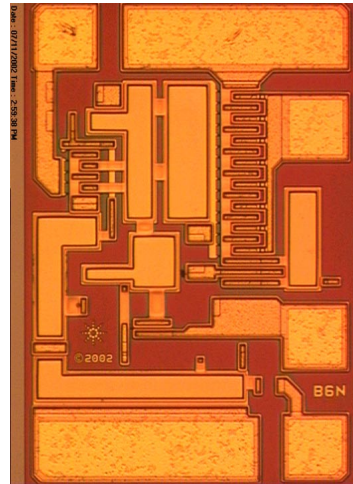


Figure 3. Die Layout.

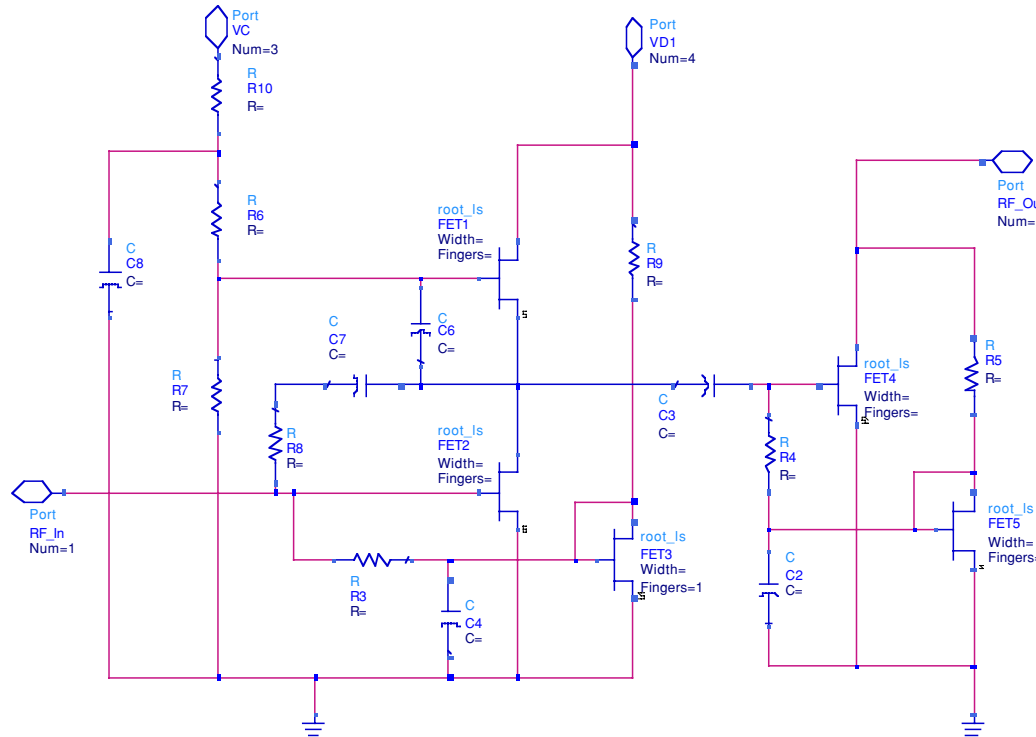
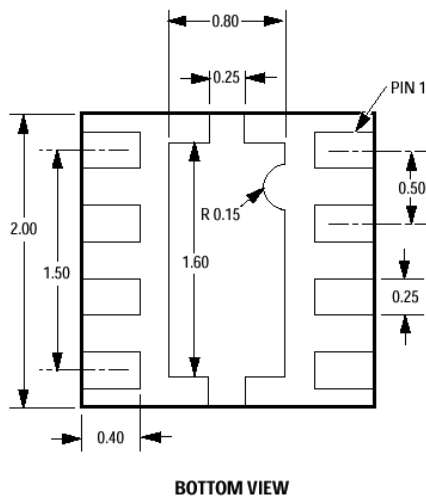


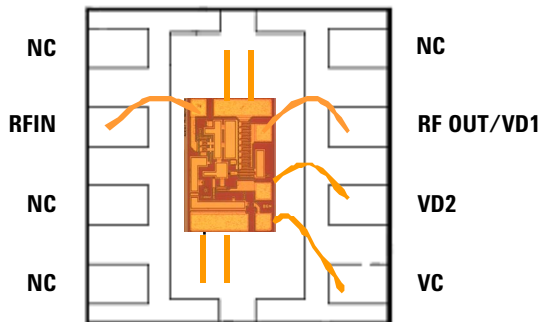
Figure 2. Designed Circuit.

Figure 4a shows the LPCC 2x2 package outline drawing and dimensions. The exposed die-attach paddle serves as device ground and heat dissipation path, and to reduce the package lead inductance. Additionally, a pair of exposed tie bars enables visual and electrical confirmation of solder joints between the die-attach paddle and printed circuit board. The package is compliant with EIA/JEDEC moisture sensitivity level 1 (MSL1) lead free profile.<sup>[3]</sup>

Figure 4b shows the bonding diagram for the chip. Multiple ground pins are used to reduce bond wire parasitic inductances, which would otherwise reduce the gain of the circuit.



4a: Bottom View of LPCC 2x2 Package



4b: Top View of LPCC 2x2 Package

Figure 4: LPCC 2x2 Package Outline Drawing and Dimension (in mm) with the IC inside.

## Packaged Measured Results

The packaged device was evaluated using the circuit shown in Figure 5. Figure 6 shows a picture of the actual test board on 10mil thick FR4. A 12nH inductor serves as an RF choke for the DC supply line Vd2. The resistance value of Rbias at pin 7 can be varied to get the required saturated power and to save current.

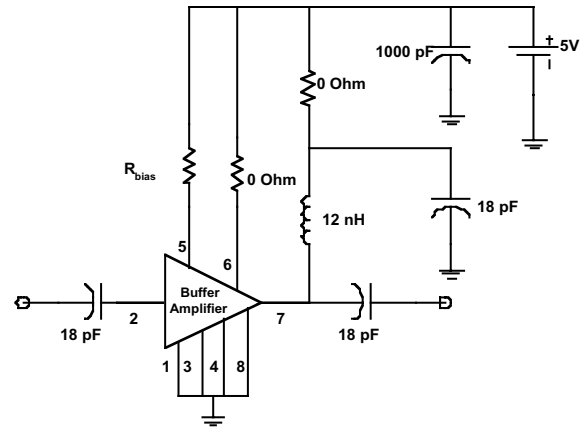


Figure 5. Evaluation circuit.

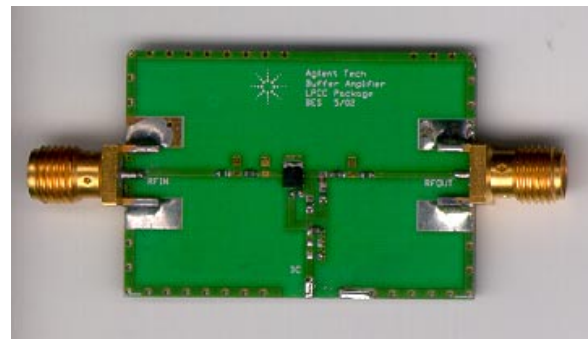


Figure 6. Evaluation board.

The buffer amplifier is internally matched at 2 GHz. Figure 7 shows its small signal performance measured in a 50-ohm system. Typical input and output return losses measured at the board level are 10 dB and 13 dB respectively at 2 GHz. If better impedance matching is required, an L-C matching network can be utilized at the input. Changing these component values can achieve the optimum matching conditions at different frequencies. Reverse isolation is better than 40 dB across the band from 0.5–6 GHz. Small signal gain is 23 dB at 2 GHz.

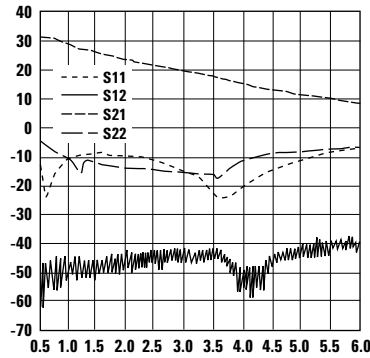


Figure 7. S-parameters in a 50-ohm system.

Figure 8 shows the plot of Psat versus Rbias for 5V and 3V operation at 2 GHz. The higher the Rbias (its location is shown in Figure 5), the more voltage limited the second stage will become. This reduces the saturated power and also saves current. With an Rbias of 0 Ohm, the device drains approximately 65 mA of current from a 5V source and approximately 42 mA from a 3V source at saturated power level. Figure 9 shows the plot of Id. vs. Psat. Table 1 shows the measured performance summary of the device.

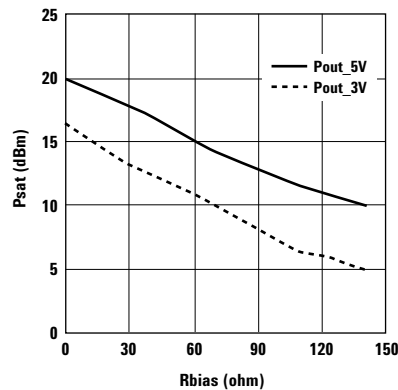


Figure 8. Psat vs. Rbias for 5V and 3V at 2 GHz.

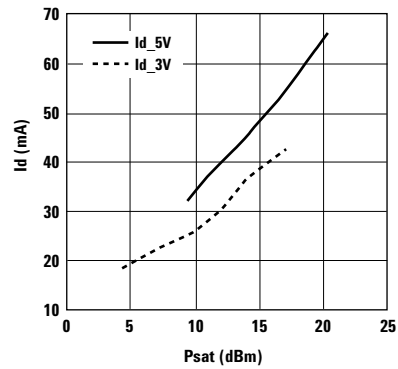


Figure 9. Id vs. Psat for 5V and 3V at 2 GHz.

Table 1. Performance Summary at 2 GHz

Parameter		Unit	Design	
Sz	Dies Size	μm	700x500	
Pkg	Package Type	—	2x2-8L	
Fq	Frequency Range	MHz	500-6000	
Vd	Supply Voltage	V	5	
Iq	Quiescent Current	mA	45	
Psat	Saturated Power at 0 dBm Pin	dBm	21	
ISL	Isolation	dB	40	
RL	Return Loss	Port 1	dB	-8
		Port 1	dB	-10
Ga	Gain	dB	21	

## Conclusion

The design, implementation and measured performance of a high isolation buffer amplifier have been described. Fabricated on Avago Technologies' enhancement-mode pHEMT process, this buffer amplifier uses a 2-gain stage topology and can achieve better than 40 dB of input-output port isolation from 0.5 to 6 GHz. With a single 5V power supply at 2 GHz, it can deliver maximum output power up to 20 dBm and consumes 65 mA at 0 dBm input power. It offers a variable gain solution to save current consumption using an external bias resistor. The low-profile 2 mm x 2 mm plastic package and matched input and output ports help to reduce part count and PC board space. These features are ideal for driving a passive mixer LO port from a VCO where high reverse isolation is required by the VCO.

## Acknowledgment

We would like to acknowledge Julie Kessler for IC layout guidance and lessons. Tan Thong-Lin and Lee Hang-Kiong for advise on the Avago-VEE test program generation.

## References

- [1] Julie Kessler et al, "Low Noise Enhancement Mode PHEMT FETs for Low Cost Commercial Applications", Wireless Symposium, 2001.
- [2] Der-Woei Wu et al, "An Enhancement-Mode PHEMT for Single Supply Power Amplifiers", The Hewlett-Packard Journal, pp39-51, February 1998.
- [3] Avago Technologies, "LPCC2x2 Package", Application Note 1316.

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